ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Department of Information Technology
and Electrical Engineering

An Efficient Incremental Redundancy Implementation for 2.75G Evolved EDGE

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Outline

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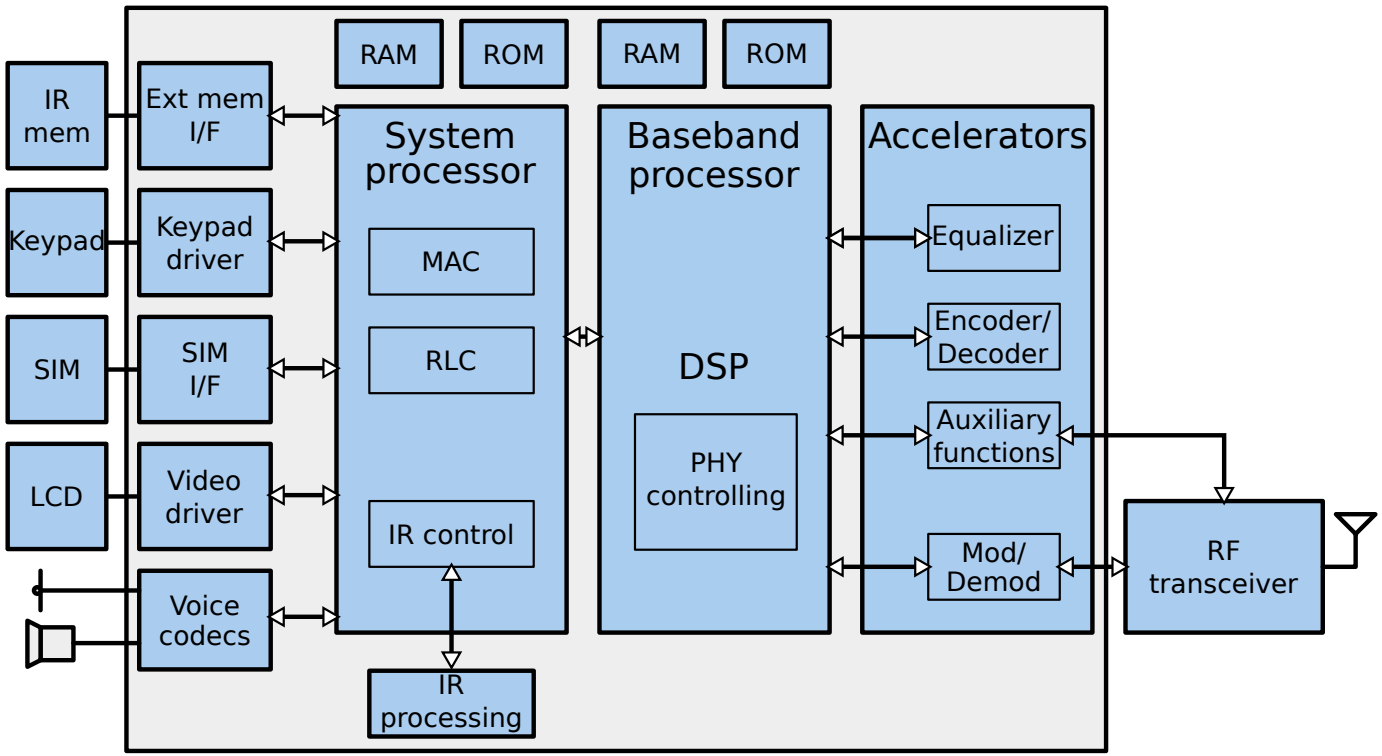
Motivation - Typical GSM Protocol Stack



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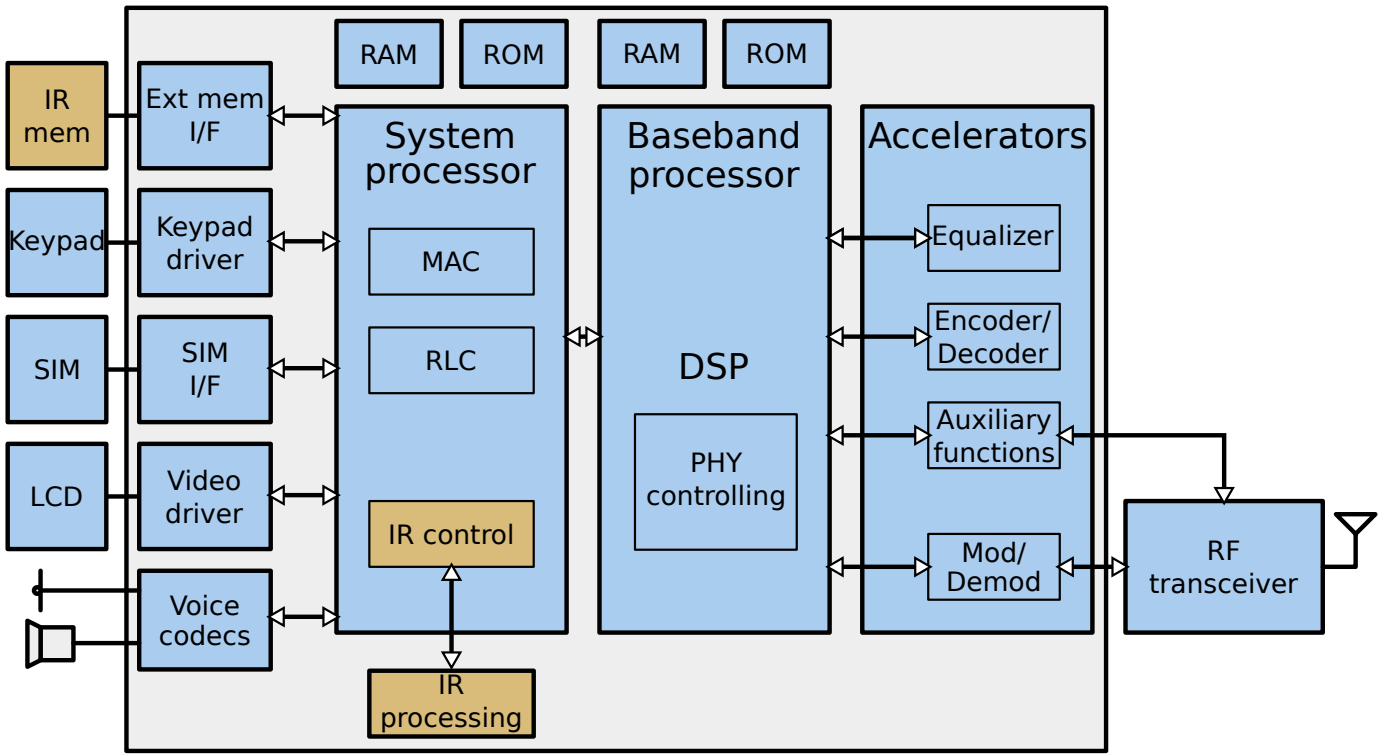

Incremetal Redundancy scattered accross components

Motivation - Vision

- Future applications
  - Machine-to-Machine (M2M) communication
  - Internet of Things (IoT)
- Single chip Physical Layer (PHY)
  - No external components
  - Less cross-layer traffic
- Simple layer 2 and layer 3 design $\rightarrow$ software

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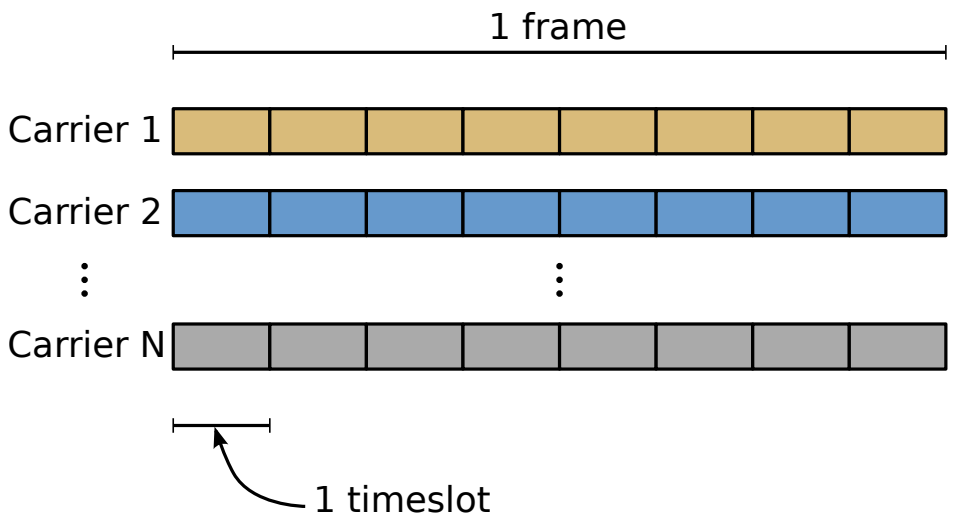
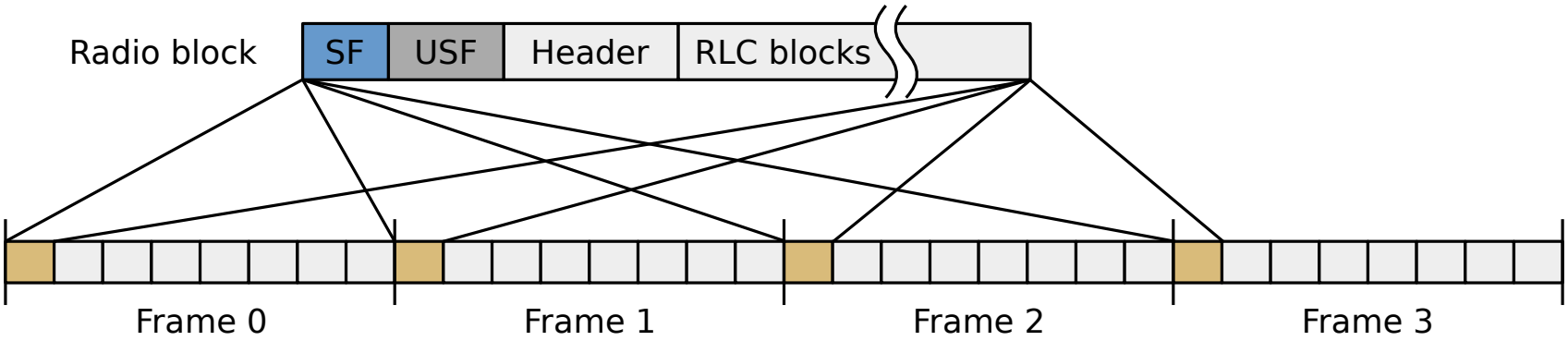
GSM Specifications - Basics

- Physical channel division with TDMA and FDMA
- Logical channel maps to timeslots on physical carrier
- 8 timeslots form a frame
- 116 information symbols per burst (timeslot)
- Basic operation mode
  - Full rate voice channel
  - GMSK
  - 13 kbit/s



GSM Basics - Packet Data Channels

- Multislot classes (up to 6 timeslots)
- GPRS: GMSK, 21.4 kbit/s per timeslot
- EGPRS: 8-PSK, 59.4 kbit/s per timeslot
- EGPRS-2: 16-QAM, 32-QAM, 98.7 kbit/s per timeslot
- Radio block:
  - Stealing Flag (SF)
  - Uplink State Flag (USF)
  - Header
  - RLC blocks (payload)



GSM Specifications - Incremental Redundancy

- Joint operation of PHY and layer 2 (RLC/MAC)
- Subset of Hybrid ARQ

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Uncoded RLC block 

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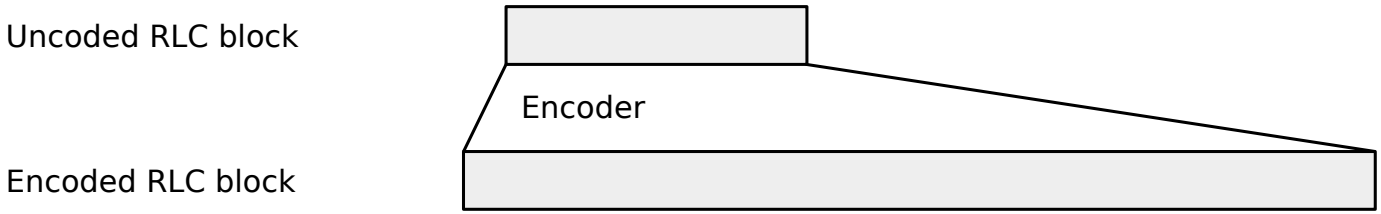

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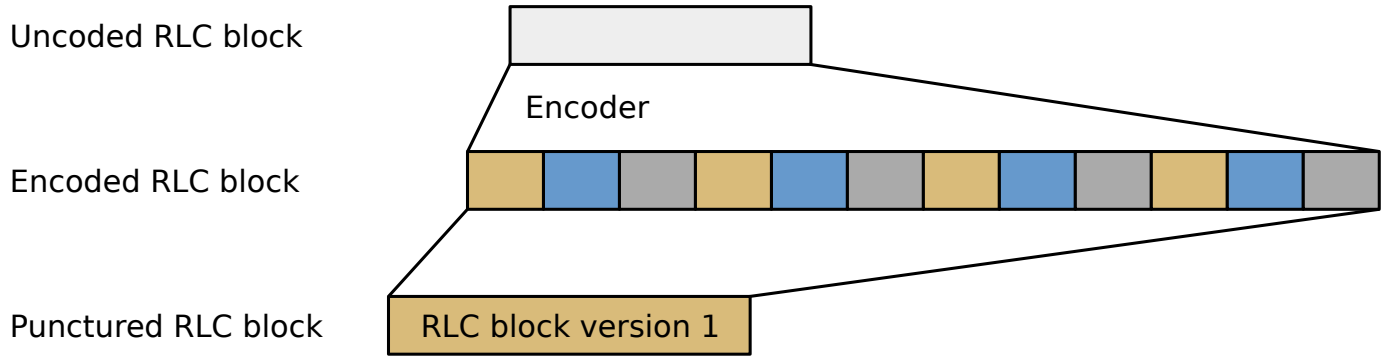

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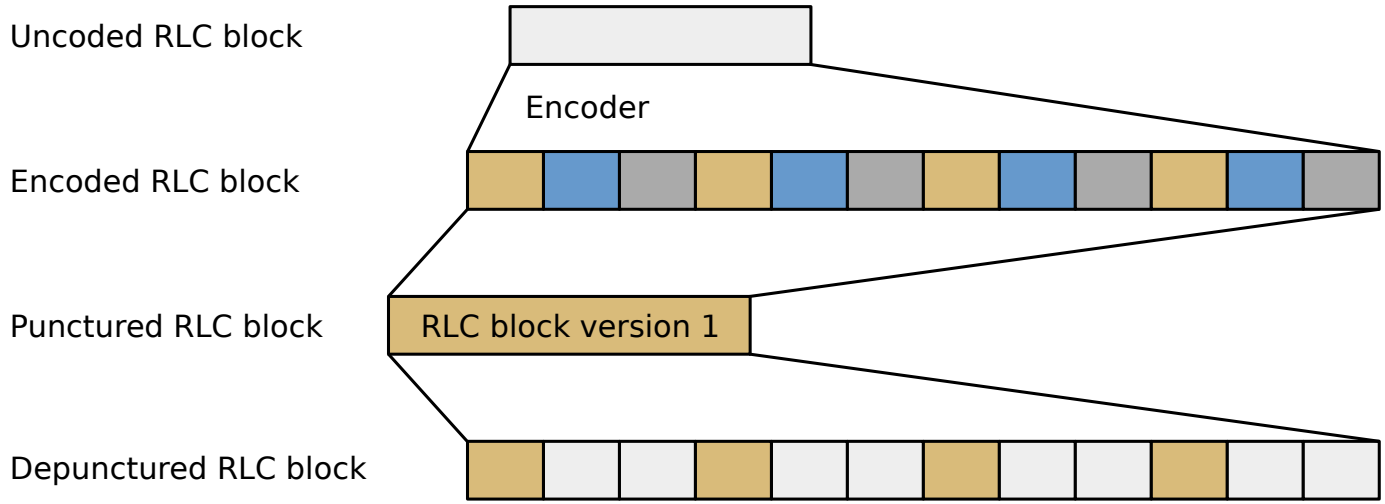

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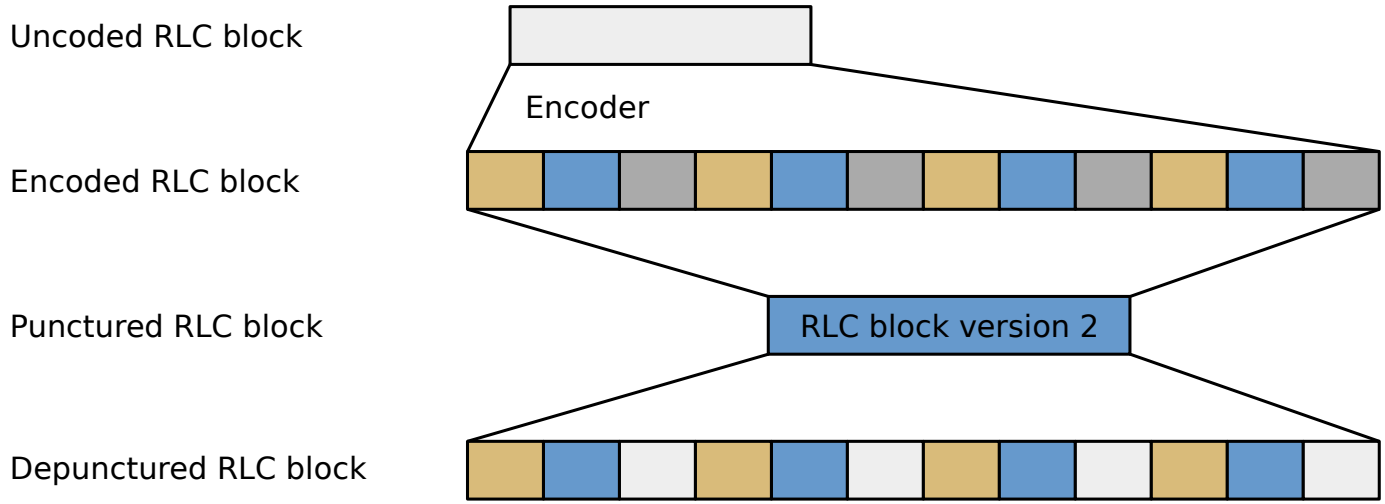

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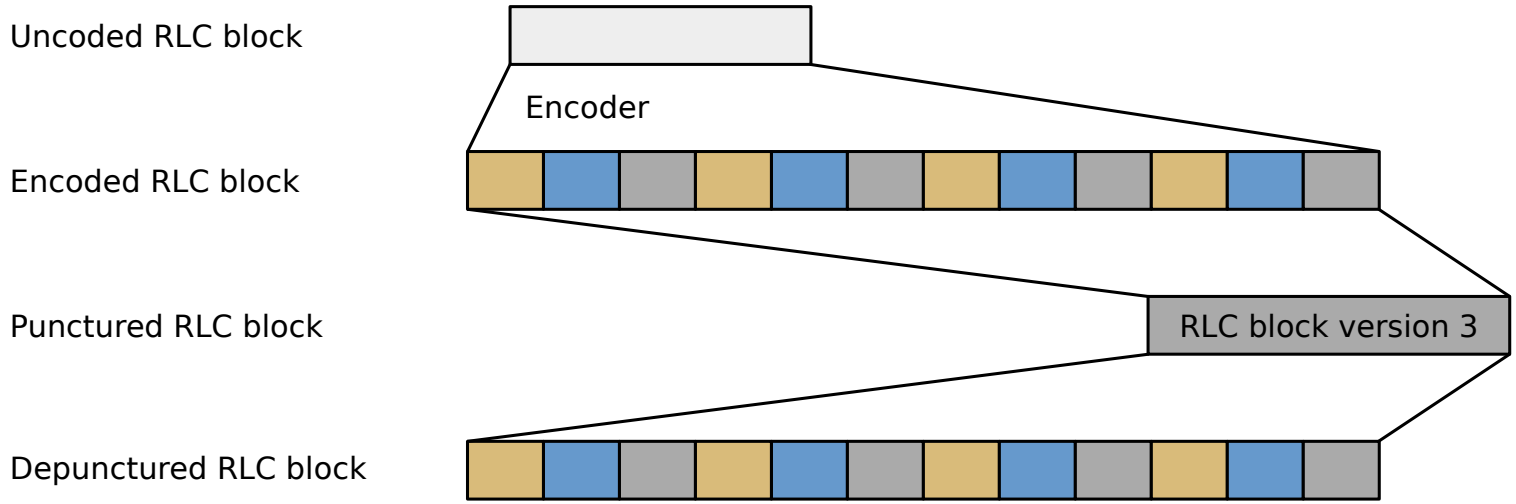

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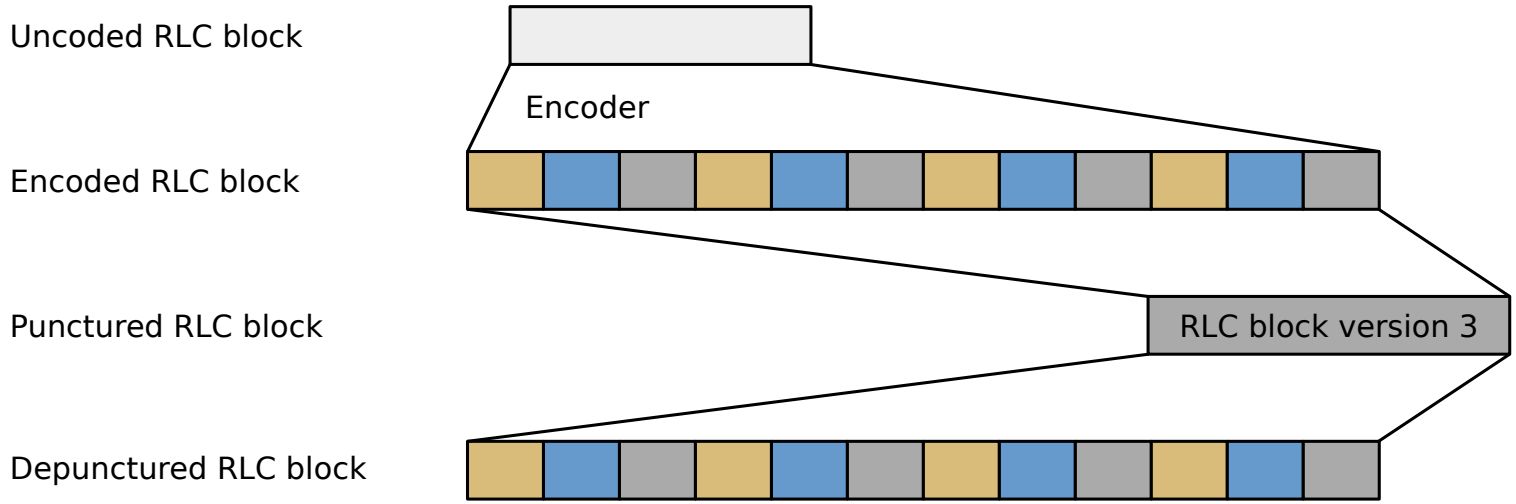

- Specifications: minimum throughput with IR enabled

  $\rightarrow$ Simulations: evaluate minimal memory size

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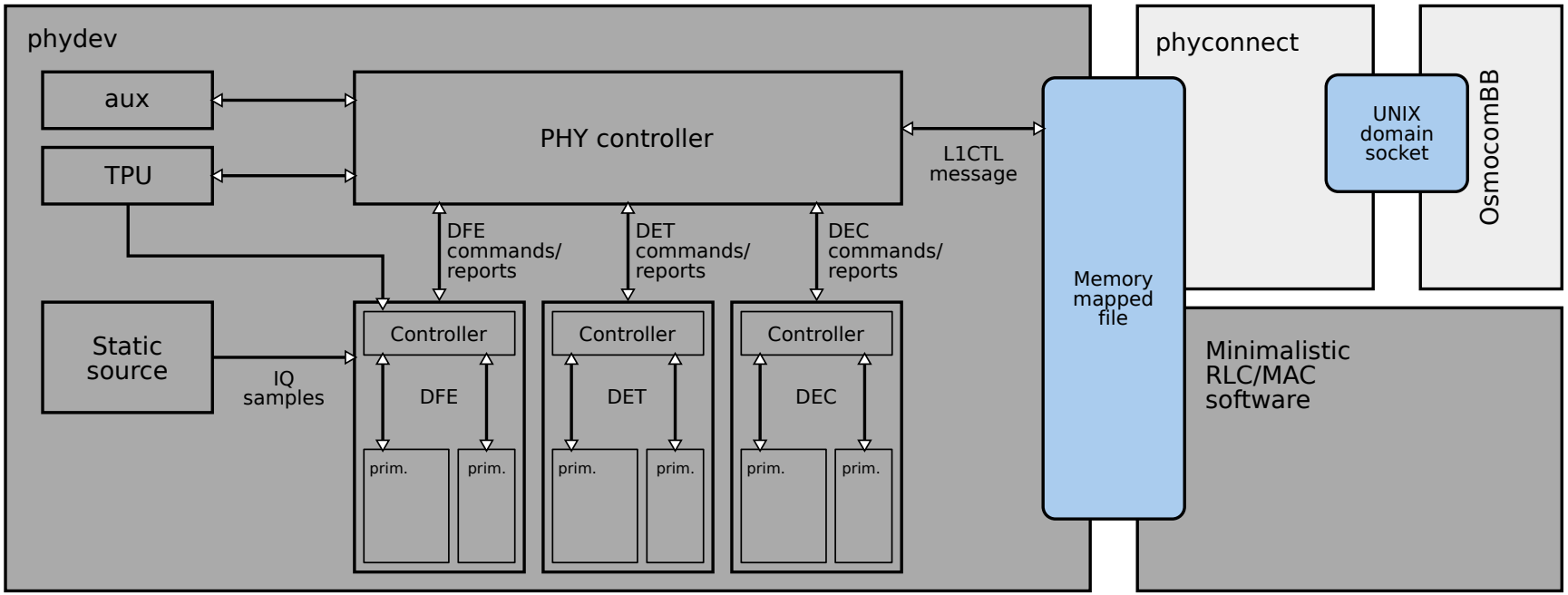
MatPHY - An Open Source GSM/EDGE PHY Framework



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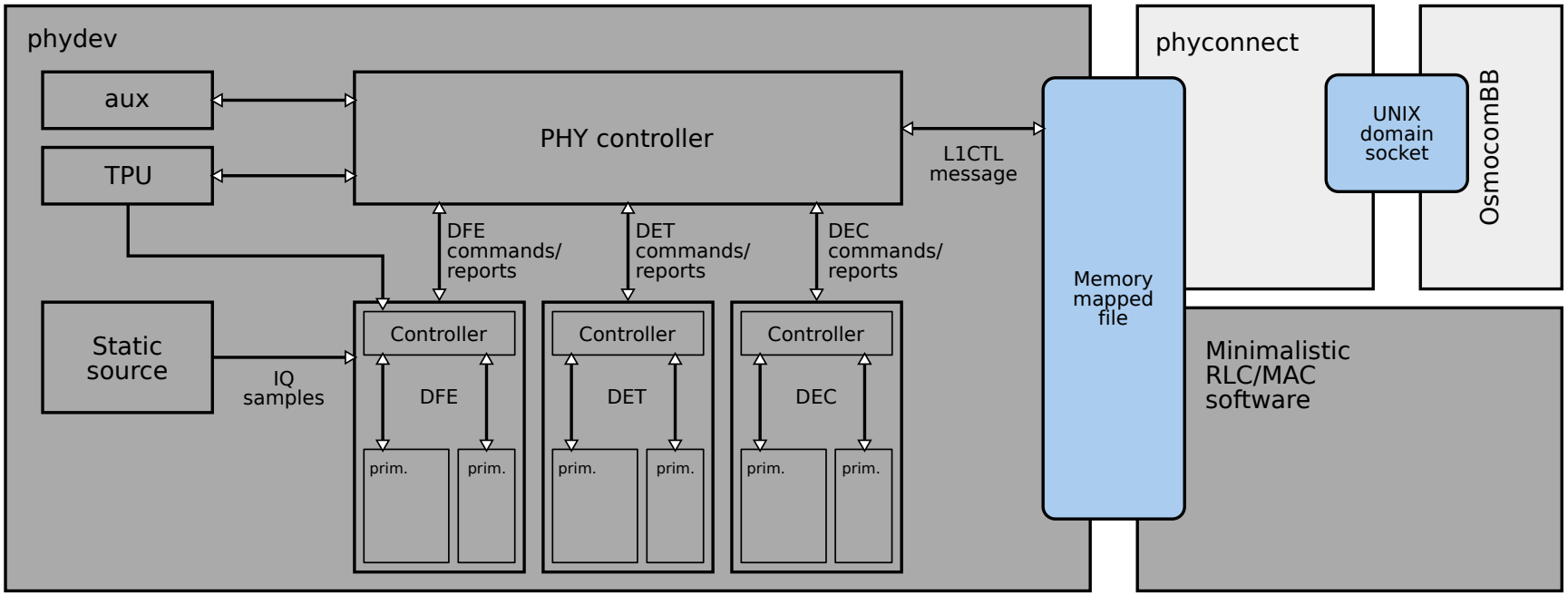
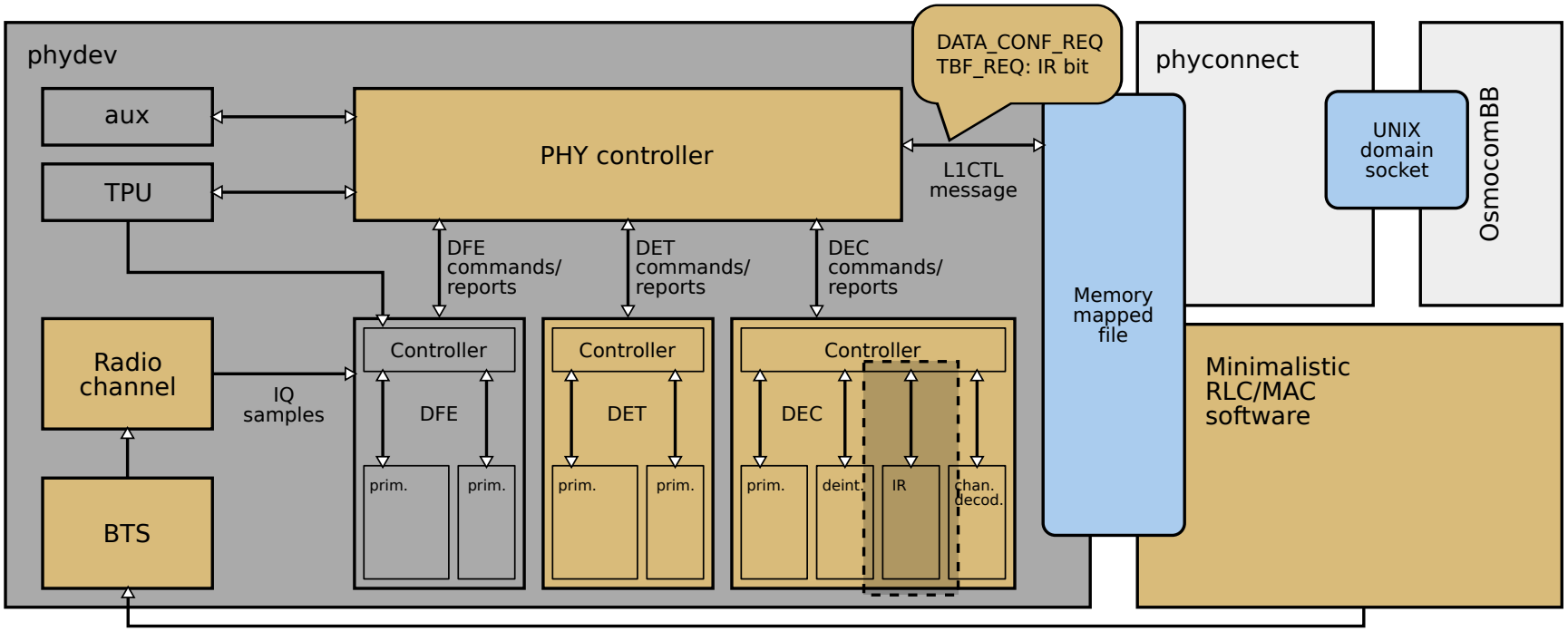


Evolved EDGE support:

- Modulation and coding schemes → DET, DEC
- L1CTL enhancement → Evolved EDGE support
- Configurable data source → Base Transceiver Station (BTS)

MatPHY - Extensions



- Straight forward IR in DEC
- Infinite memory
- Block Error Rate (BLER) depending on retransmission count

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Performance Evaluation - Setup

- Parallel simulations with MatPHY
  - Entire receiver
  - Noise Figure (NF)
  - Infinite IR memory
  - BLER depending on retransmission

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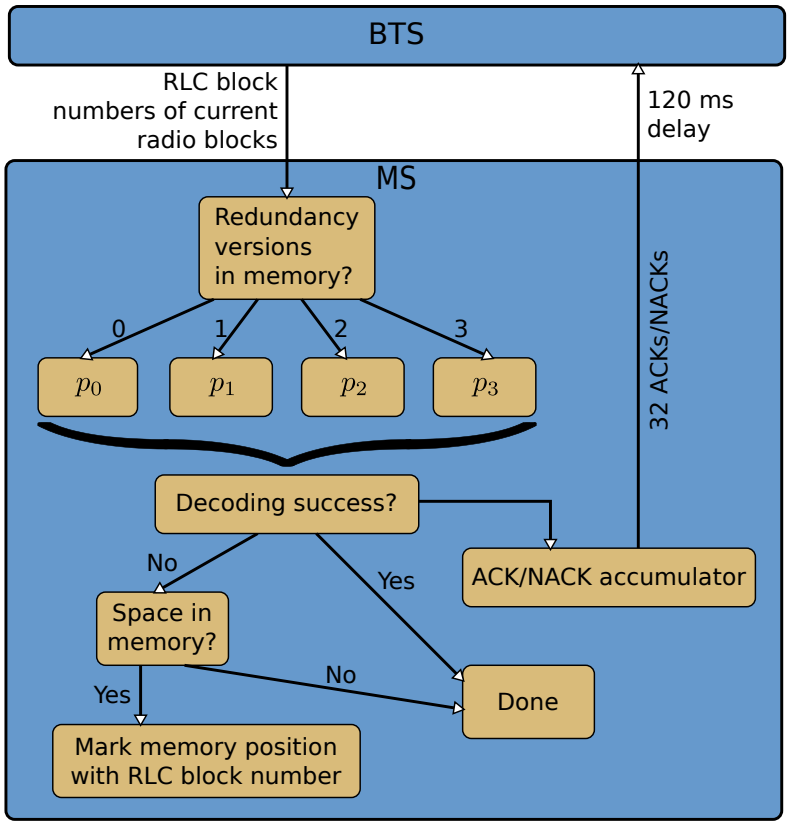
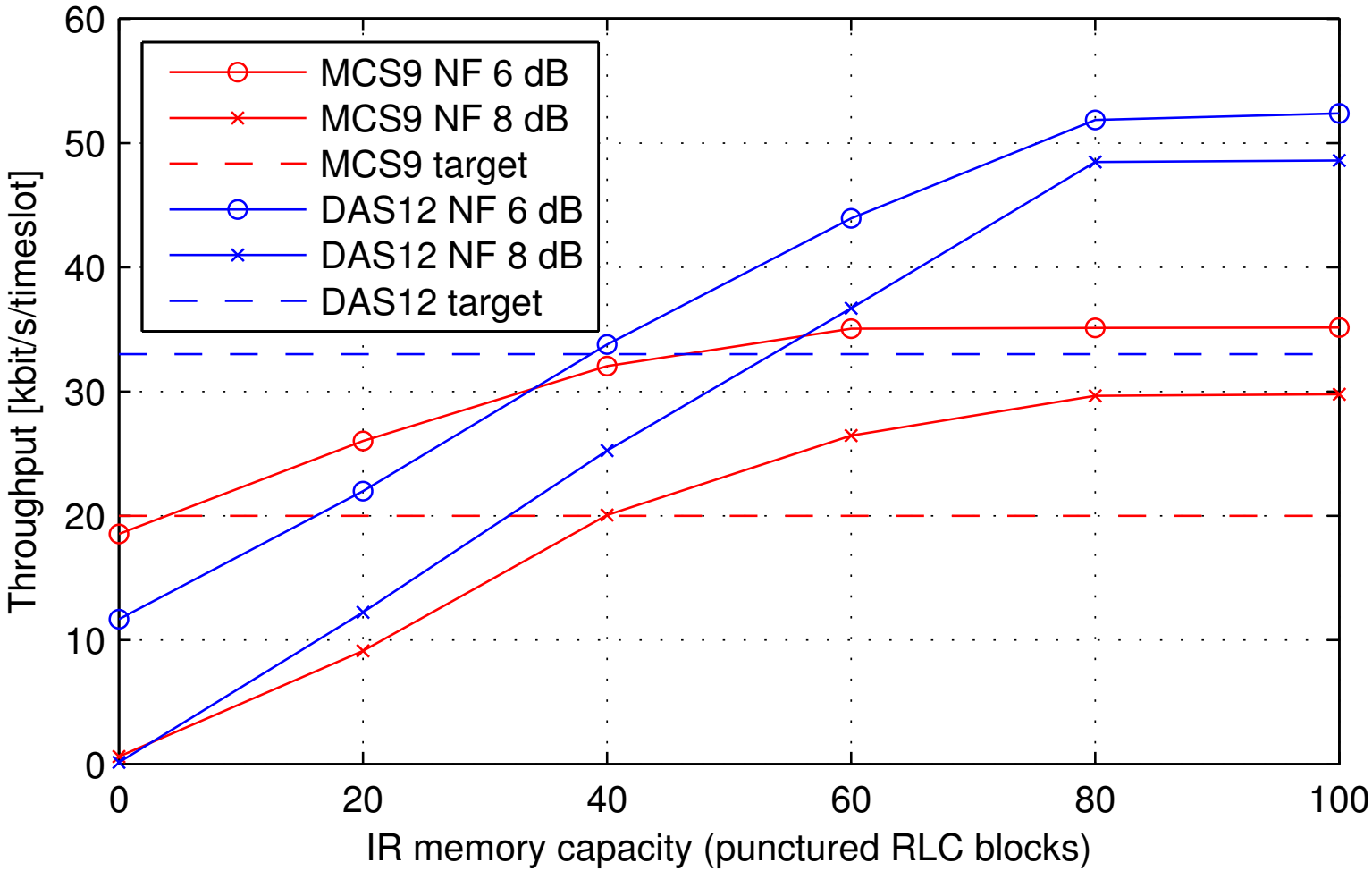


- Parallel simulations with MatPHY
  - Entire receiver
  - Noise Figure (NF)
  - Infinite IR memory
  - BLER depending on retransmission
- Sequential simulation:
  - No PHY operations $\rightarrow$ fast
  - IR memory size as parameter
  - Specifications for IR test case
  - RLC/MAC procedures
  - Round-trip time
  - Flow control

Results of Performance Evaluation



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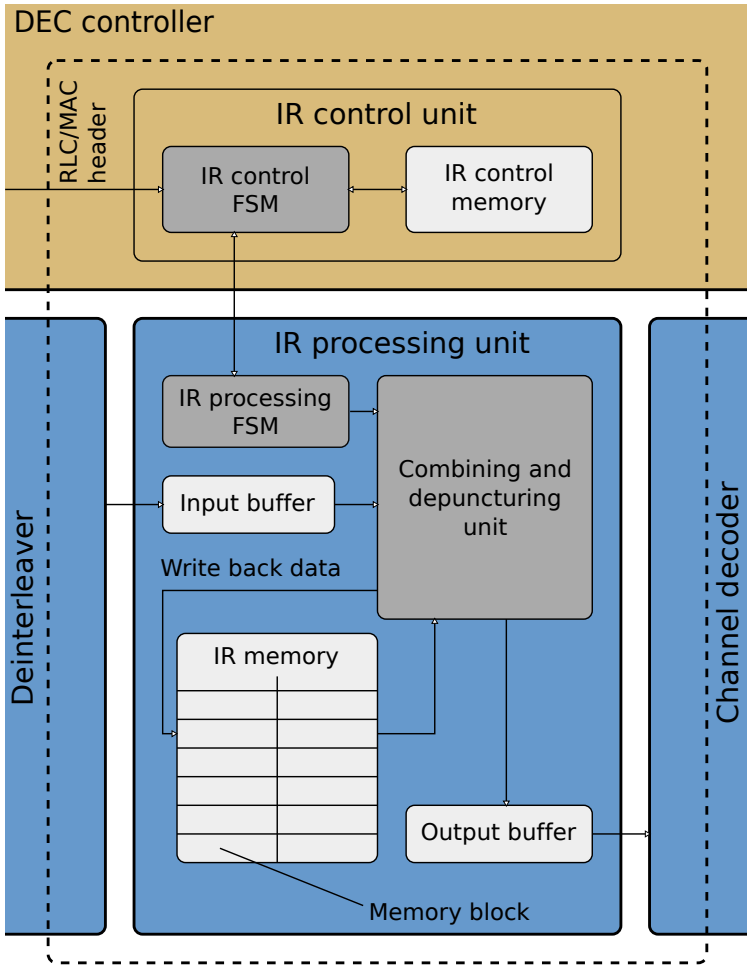
Dedicated Hardware Architecture - Proof-of-Concept



- Hardware description language and on-chip memory
- IR processing unit between deinterleaver and channel decoder
- Control memory: identify RLC blocks
- Input buffer, output buffer
- IR memory fragmented into blocks

Synthesis and Clocking

- Sample IR memory size: $2^{15} > 46 \times 658$ soft value
- Sample soft value width: 5 bits
- Implemented in VHDL
- Synthesized using a 130nm CMOS technology
- Maximum clock frequency 187 MHz corresponding to 50k Gate Equivalents (GE)
- Memory sizes:

Memory	Soft values	Size (kbit)
Control memory	N/A	2.438
Input buffer	1248	6.24
Output buffer	2022	10.11
IR memory	32768	163.84
Total memory	36038 (without control)	182.628

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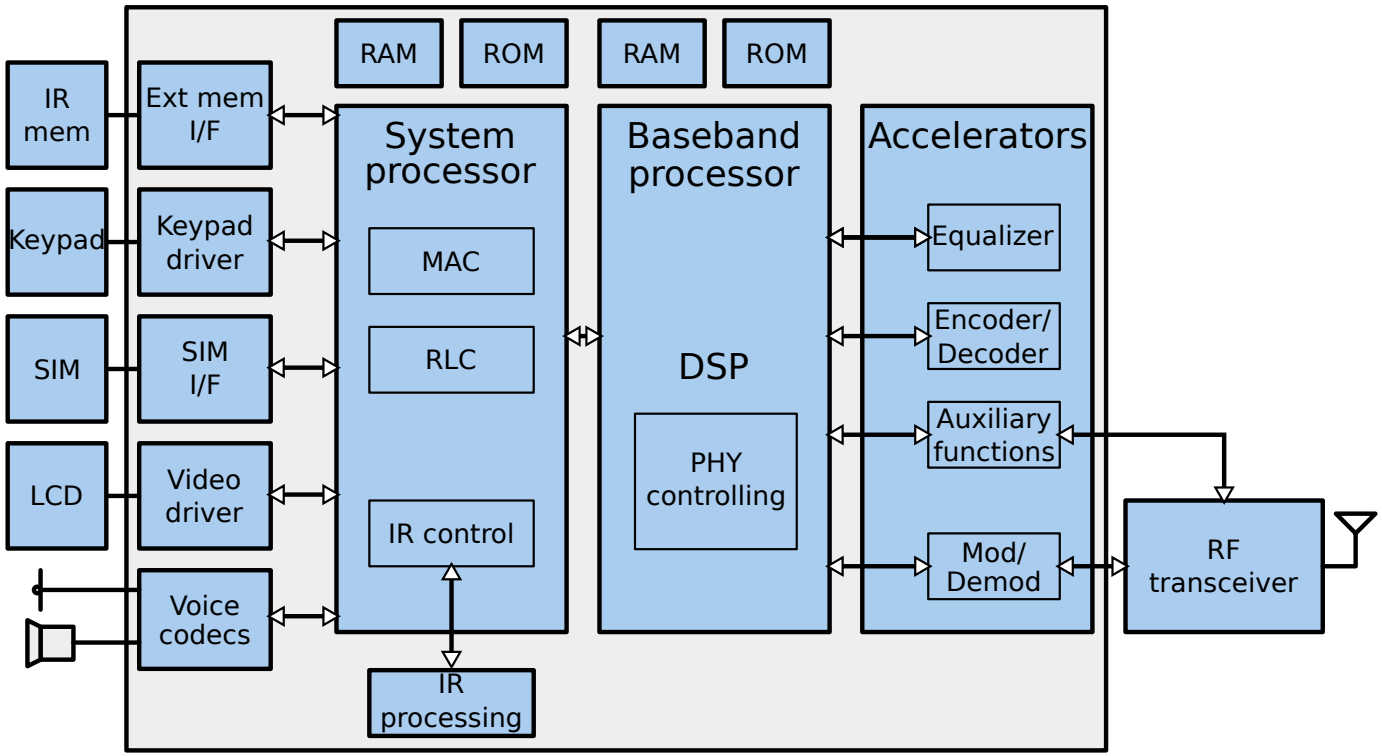

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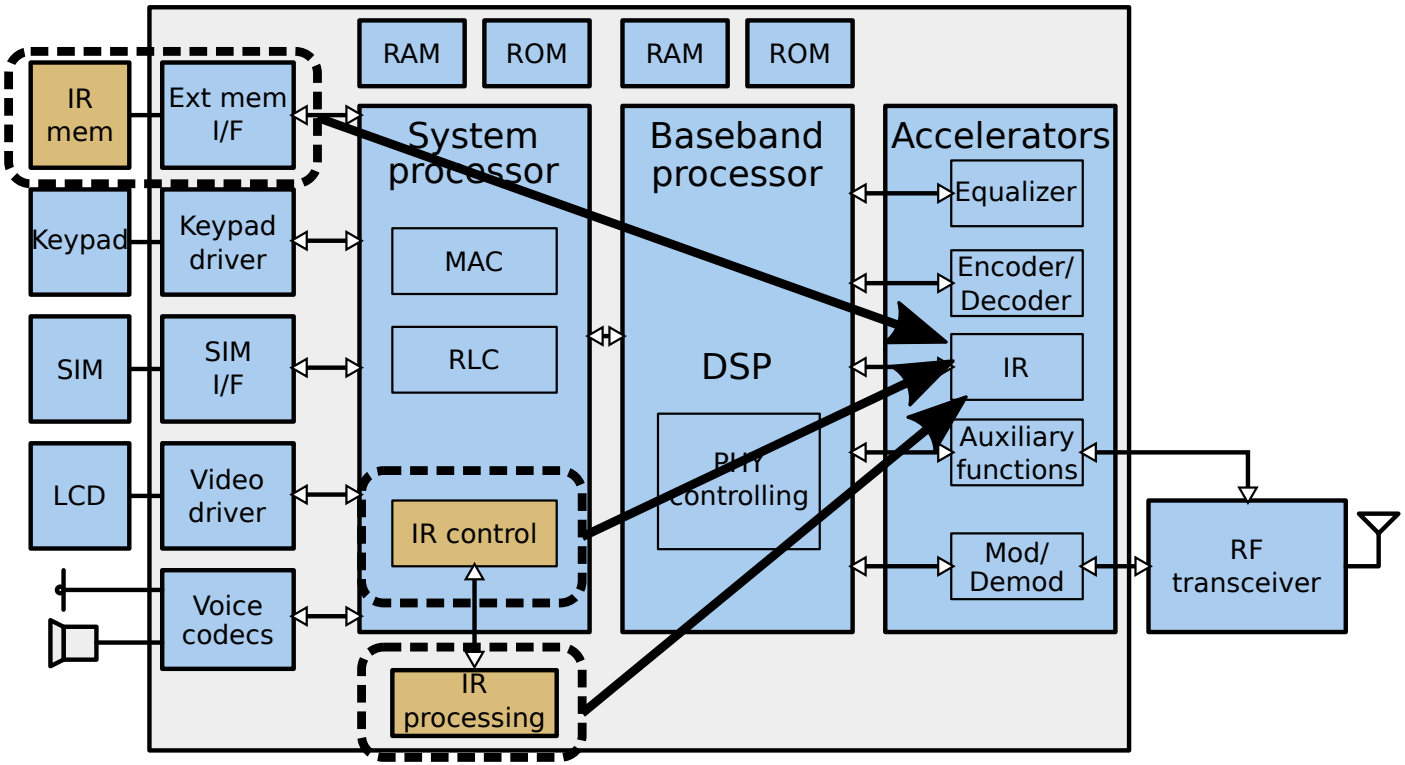

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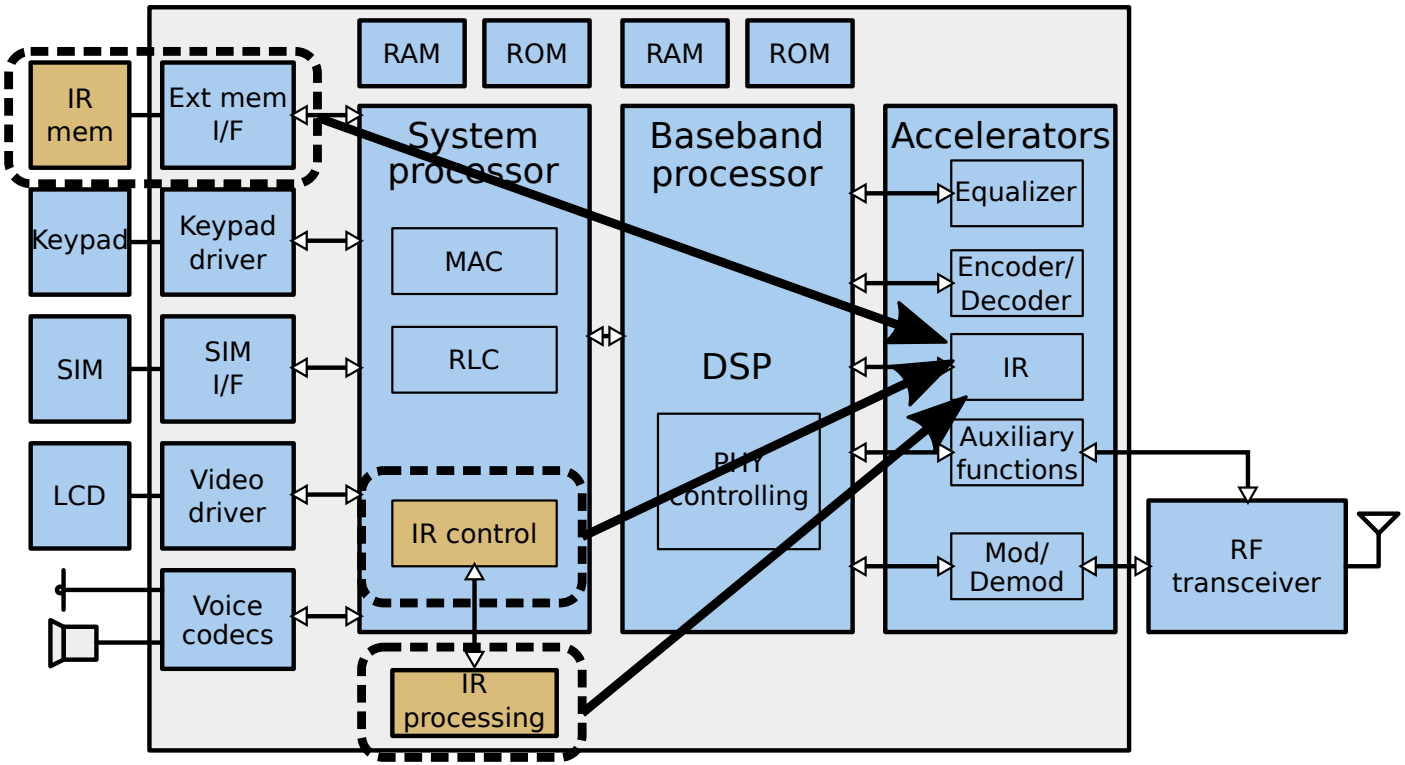

Thank you for your attention